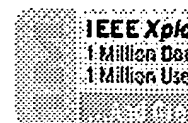
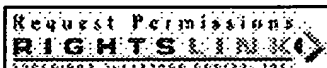



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Processor-based built-in self-test for embedded DRAM

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Abstract:

A built-in self-test engine and test methodology have been developed for testing a fa of high-bandwidth, high-density DRAM macros. The DRAM macros range in size from 256×16×128 to 2 K×16×256 (Word×Bit×Data) and are targeted for embedded applications in application-specific integrated circuit designs. The processor-based te engine, with two separate instruction storage memories, combines with flexible addr data, and clock generators to provide DRAM high-performance ac testing using a minimum of dedicated test pins. Test results are compressed through on-macro, two dimensional, redundancy allocation logic to provide direct programming information i the fuser via a serial scan port. The design is intended for reuse on future DRAM-generation subarrays and can be adapted to any number of address or data-pin configurations

Index Terms:

[application specific integrated circuits](#) [built-in self test](#) [integrated circuit testing](#) [memory architecture](#) [random-access storage](#) [redundancy](#) [DRAM-generation subarrays](#) [application-specific integrated circuit designs](#) [built-in self-test engine](#) [clock generators](#) [data-pin configurations](#) [dedicated test pins](#) [direct programming information](#) [embedded DRAM](#) [high-d](#) [DRAM macros](#) [instruction storage memories](#) [processor-based built-in self-test](#) [redundancy allocation logic](#) [serial scan port](#) [test methodology](#)

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